REMARKS

This paper is being provided in response to the Office Action mailed October 28, 2004, for the above-referenced application. In this response, Applicant has cancelled claims 19-21, 27, 28, 30 and 31 (claims 1-14, 16-18 and 25-26 having been previously cancelled) without prejudice or disclaimer of the subject matter thereof, and amended claims 15 and 22 and added new claim 32 to clarify that which Applicant considers to be the invention. Applicant respectfully submits that the amendments to the claims and the new claim are fully supported by the originally-filed specification.

The rejection of claim 15 under 35 U.S.C. 102(b) as being anticipated by JP 96-208790 to Takashima (hereinafter "Takashima") is hereby traversed and reconsideration is respectfully requested.

Independent claim 15, as amended herein, recites a delay circuit for delaying a logic signal having two logic levels consisting of a low level and a high level. The delay circuit includes an inverter chain containing not less than four inverters. A p-channel MOS transistor and an n-channel MOS transistor comprise each of the at least four inverters, and wherein a gate threshold voltage of each gate of said p-MOS and n-MOS transistors is shifted in mutually opposing directions. Low threshold voltage n-MOS transistors of each of a first and a third inverter are connected to ground by a high threshold n-MOS transistor. Low threshold voltage p-MOS transistors of each of a second and a fourth inverter are connected to a power source line by a high threshold voltage p-MOS transistor. When an input logic signal is fixed at a low level during a standby state, the high threshold voltage n-MOS transistor is set to an off-state in

response to a chip select signal controlling the standby state, and the high threshold voltage p-MOS transistor is set to an off-state in response to the chip select signal that is negated.

The Takashima reference discloses a semiconductor device for sustaining high speed operation while suppressing stand-by current even when a low voltage internal power supply is employed by setting a threshold for a MOS transistor and setting the power supply variably at the time of stand-by. The Office Action cites Figure 8 of Takashima in which is disclosed a four inverter step delay circuit and Figure 10 illustrates clock signals phi 1 and phi 2 in operation with respect to signals Vcc1 and Vss1.

Applicant respectfully submits that Takashima does not teach or fairly suggest all of the above-noted features as claimed by Applicant. Applicant's present claimed invention recites at least the features that a gate threshold voltage of each gate of the n-MOS and p-MOS transistors is shifted in mutually opposing directions. As a result, Applicant has found that in a delay circuit structure utilizing MOS transistors or capacitors having the above-noted features, generation of leak current during the standby state is suppressed and thereby source-voltage dependency of the delay time is contained and power consumption is effectively controlled during the standby state. (See page 32, lines 2-14 of the present application.) In contrast, Takashima does not disclose or suggest these features as claimed by Applicant and that provide the above-noted desirable effects.

Furthermore, Applicant's independent claim 15 recites at least the features of a delay circuit comprising first and second inverters and first and second capacitors, coupled as noted above, wherein, when a logic signal is fixed at a low level during a standby state, one of said first

capacitor and said second capacitor is set to an off-state in response to a chip select signal controlling said standby state, and the other of said first capacitor and said second capacitor is set to an off-state in response to said chip select signal that is negated. The Office Action cites the signal phi 1 (shown in Fig. 10 of Takashima) as a chip select signal controlling the standby state. A second signal phi 2 appears to be a second chip select signal, but it is not strictly a negation of phi 1 as can be seen by the falling and rising edges of the phi 1 and phi 2 signals shown in Fig. 10(b) of Takashima. On the other hand, instead of two separate chip select signals, Applicant recites that the two capacitors, noted above, are controlled by a chip select signal and, specifically, a negated chip select signal in setting the off-states of the two capacitors.

Accordingly, Applicant submits that Takashima does not teach or fairly suggest a delay circuit having the above-noted features as claimed by Applicant. In view of the above, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

The rejection of claims 20, 27, 28 and 31 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,825,698 to Kim et al. (hereinafter "Kim") has been rendered moot by the cancellation of claims 20, 27, 28 and 31 herein.

The rejection of claims 22 and 23 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,115,146 to McClure (hereinafter "McClure") is hereby traversed and reconsideration is respectfully requested in view of the amendments to the claims contained herein.

Independent claim 22, as amended herein, recites a delay circuit including first, second and third nodes. A first inverter receives a logic signal and the output of the first inverter is coupled to the first node. A second inverter is included whose input is coupled to the first node and whose output is coupled to the second node. A third inverter is included whose input is coupled to the second node and whose output is coupled to the third node. A fourth inverter is included whose input is coupled to the third node. A first capacitor includes two electrodes, one of the electrodes connecting to a first power source line and the other connecting only to the first node, the first capacitor being a first transistor of a first channel type. A second capacitor is coupled between the third node and the first power source line, the second capacitor being a second transistor of the first channel type. Claims 23 and 24 depend from independent claim 22.

The McClure reference discloses a power-on reset circuit for controlling test mode entry. The Office Action refers to the inverter chain and capacitors shown in Figure 1 of McClure.

Applicant respectfully submits that McClure does teach or fairly suggest the above-noted features as claimed by Applicant. Specifically, the Office Action cites Figure 1 (see also Figure 2) of McClure is which is illustrated an inverter chain (elements 12 or elements 72 of Fig. 2)), two capacitors (elements 50 and 74 of Fig. 2) connected between nodes of the inverter chain and a power source line Vcc, and a transistor (element 52 of Fig. 2) connected to a node between capacitor 50 and the inverter chain. Applicant submits that McClure does not identify the capacitors 50 and 74 as transistors of a first channel type, as is claimed by Applicant, and discloses only one transistor 52 connected to the third node. Further, Applicant recites that one electrode of the first capacitor is connected only to the first node. In contrast, the capacitor 50 of McClure is connected not only to the node between invertors but also to the transistor 52.

Accordingly, in view of the above, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

The rejection of claims 22 and 24 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,055,713 to Watanabe et al. (hereinafter "Watanabe") is hereby traversed and reconsideration is respectfully requested.

The features of independent claim 22 are discussed above. Claim 24 depends therefrom.

The Watanabe reference discloses an output circuit of an integrated circuit including first and second MOS transistors and a drive and control circuit. In Fig. 5, Watanabe discloses two inverters (I2 and I3), two capacitors (C1 and C2) and power source lines (VSS and VCC) with an output directed to a logic gate (a NAND gate-NA1); and in Figs. 7 and 11, Watanabe discloses the delay circuit with four inverters, two capacitors and a NOR gate NG.

Applicant respectfully submits that Watanabe does not teach or fairly suggest all of the above-noted features as claimed by Applicant. Specifically, the Office Action cites Figure 11 of Watanabe and directs attention to inverters I9-I11 which output to a NOR gate NG. However, Applicant recites four inverters, and thus, for Watanabe's disclosure to correspond to the claimed inverter chain structure, inverters I8-I11 of Watanabe must be considered. Consequently, the capacitors C2 and C3 of Watanabe cited by the Office Action are, in fact, connected to nodes 2 and 4 under the analysis of the Office Action and NOT nodes 1 and 3, as is recited by Applicant. Furthermore, Applicant specifically recites that no capacitor is connected to the second node.

Accordingly, Applicant respectfully submits that Watanabe does not teach or fairly suggest at least the above-noted features as claimed by Applicant and requests that this rejection be reconsidered and withdrawn.

The rejection of claims 19 and 21 under 35 U.S.C. 103(a) as being unpatentable over Takashima in view of Kim has been rendered moot by the cancellation of claims 19 and 21 herein.

The rejection of claim 29 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,672,990 to Chaw (hereinafter "Chaw") is hereby traversed and reconsideration is respectfully requested.

Independent claim 29 recites delay circuit. The circuit includes 2n+1 nodes defined in series, n being a natural number, a first node receiving a logical signal and 2n inverters, each inverter arranged between adjacent nodes of said 2n+1 nodes. A capacitor of an n-MOS type is coupled between an even node and a power source line. A NOR gate is coupled to the first node and the (2n+1)th node.

The Chaw reference discloses an edge trigger pulse generator. The Office Action cites Figure 5 of Chaw in which is disclosed an inverter chain (30a and 30b) connected to a NOR gate (30c) and a capacitor coupled between a node (between inverters 30a and 30b) and ground.

The Office Action asserts that it would be notoriously well known to substitute a MOS capacitor for a capacitor as disclosed in Figure 5 of Chaw. Applicant points out that Applicant

does not just recite that a MOS capacitor is coupled between an even node and a power source line, but rather recites that the MOS capacitor is an n-MOS type that operates accordingly in the delay circuit. (See Figure 4 of the present specification). Accordingly, Applicant respectfully submits that at least these features as claimed are not taught or suggested by the Chaw reference and respectfully requests that this rejection be reconsidered and withdrawn.

The rejection of claim 30 under 35 U.S.C. 103(a) as being unpatentable over Kim is rendered moot by the cancellation of claim 30 herein.

Further, Applicant has added new claim 32 and respectfully submits that this claim is patentable over the cited prior art.

Based on the above, Applicants respectfully request that the Examiner reconsider and withdraw all outstanding rejections and objections. Favorable consideration and allowance are earnestly solicited. Should there be any questions after reviewing this paper, the Examiner is invited to contact the undersigned at 617-248-4038.

Respectfully submitted,
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